TGA4534-SM

K-Band Power Amplifier

Product Description

The Qorvo TGA4534-SM is a K-Band Power Amplifier with integrated power detector. The TGA4534-SM operates from 17.7 – 19.7 GHz and is designed using Qorvo's power pHEMT production process.

The TGA4534-SM typically provides 34 dBm of saturated output power with small signal gain of 21 dB. Third Order Intercept is 42.5 dBm at 23 dBm SCL.

The TGA4534-SM is available in a low-cost, surface mount 28 lead 5x5 mm QFN package and is ideally suited for Point-to-Point Radio.

Lead-free and RoHS compliant

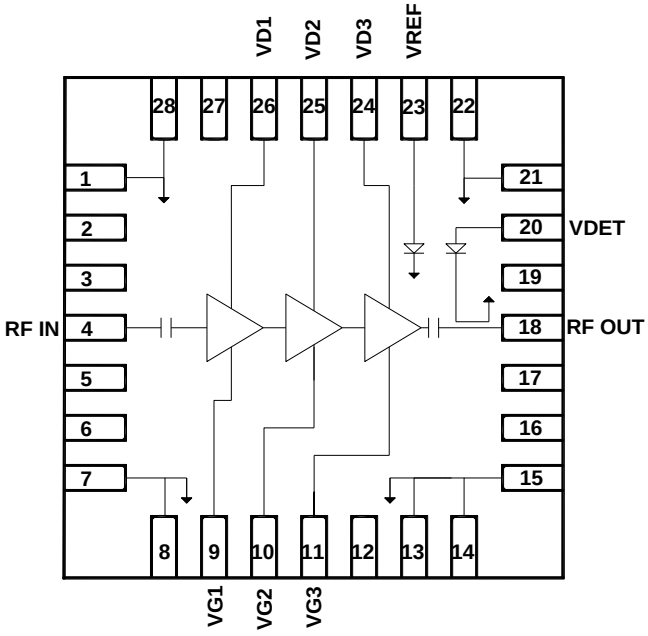
28 lead 5x5mm QFN package

Product Features

- Frequency Range: 17.7 – 19.7 GHz
- Power: 34 dBm Psat, 33 dBm P1dB
- Gain: 21 dB
- TOI: 42.5 dBm at 23 dBm/tone
- Integrated Power Detector
- Bias: Vd = 6 V, Idq = 1430 mA, Vg = -0.7 V Typical
- Package Dimensions: 5.0 x 5.0 x 1.3 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- Point-to-Point Radio
- K-band Sat-Com

Ordering Information

Part	Description
TGA4534-SM	Waffle Tray
TGA4534-SM-T/R	500 pieces on a 7" reel (standard)
TGA4534-SM EVB	Evaluation Board

Absolute Maximum Ratings

Parameter	Value
Drain to Gate Voltage, $V_D - V_G$	10 V
Drain Voltage (V_D)	6.5 V
Drain Current (I_D)	3.0 A
Gate Voltage Range (V_G)	-3 to 0 V
Gate Current (I_G)	-14 to +110 mA
Power Dissipation, P_{DISS}	20 W
RF Input Power, CW, T = 25 °C	25 dBm
Channel Temperature, T_{CH}	200 °C
Mounting Temperature (30 seconds)	260 °C
Storage Temperature	−40 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value
Drain Voltage	6 V
Drain Current, Quiescent (I_{DQ})	1430 mA
Drain Current, RF (I_{DD_Drive})	See chart page 3
Gate Voltage, Typical Range (V_G)	−0.4 to −0.8 V
Gate Current, RF (I_{G_Drive}) Typical	40 mA
Operating Temperature Range	−40 to 85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

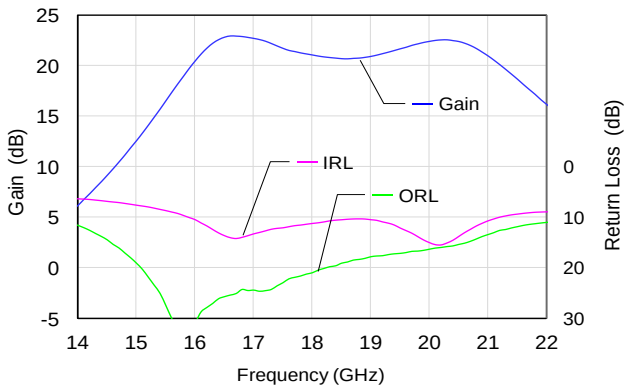
Test conditions, unless otherwise noted: 25 °C, V_D = 6 V, I_{DQ} = 1430 mA, V_G = -0.7 V typical, Z_0 = 50 Ω

Parameter	Min	Typical	Max	Units
Frequency	17.7		19.7	GHz
Small Signal Gain		21		dB
Input Return Loss		10		dB
Output Return Loss		12		dB
Output Power @ Saturation		34		dBm
Output Power @ 1 dB Gain Compression		33		dBm
Output TOI @ 23 dBm/Tone Pout/tone		42.5		dBm
Gain Temperature Coefficient		-0.02		dBm/°C
Power Temperature Coefficient		-0.005		dBm/°C

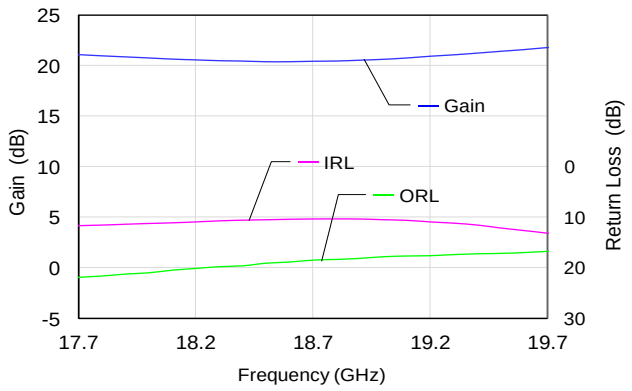
Performance Plots

Test conditions unless otherwise noted: Temp. = 25 °C, V_D = 6 V, I_{DQ} = 1430 mA, V_G = -0.7 V typical

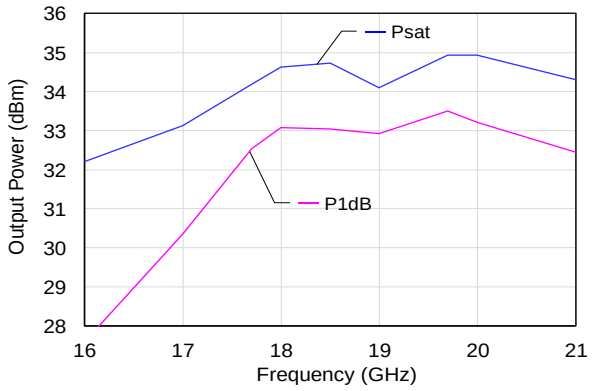
S-Parameters vs. Frequency



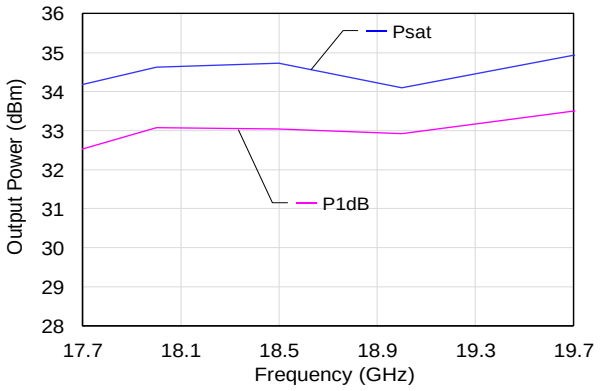
S-Parameters vs. Frequency



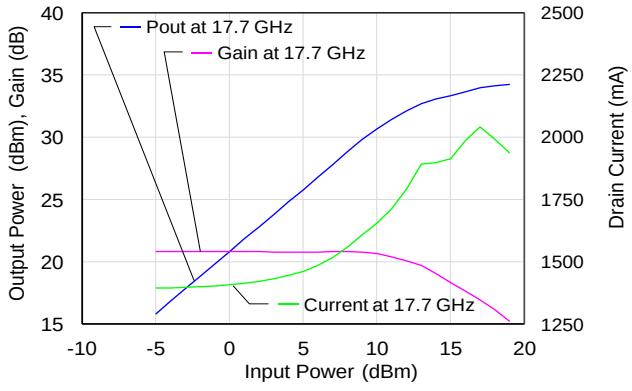
Output Power vs. Frequency



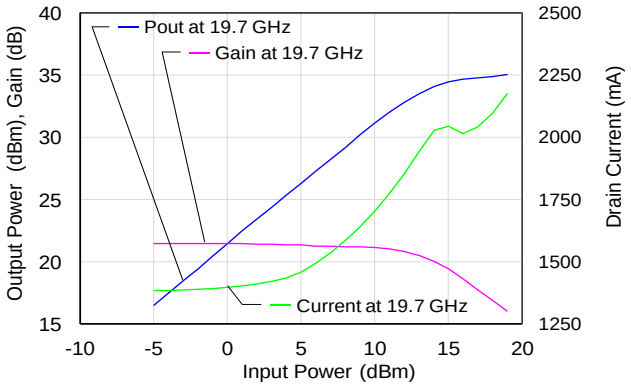
Output Power vs. Frequency



17.7 GHz Power, Gain, and Current vs. Input Power



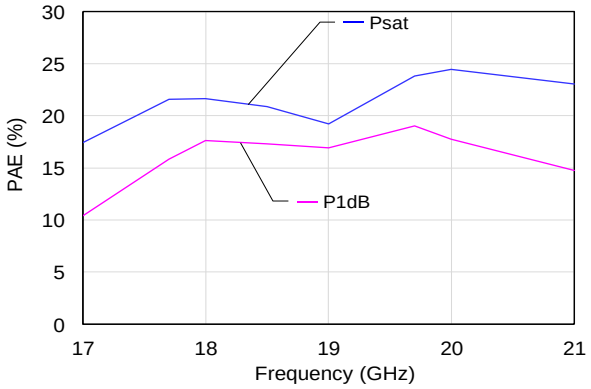
19.7 GHz Power, Gain, and Current vs. Input Power



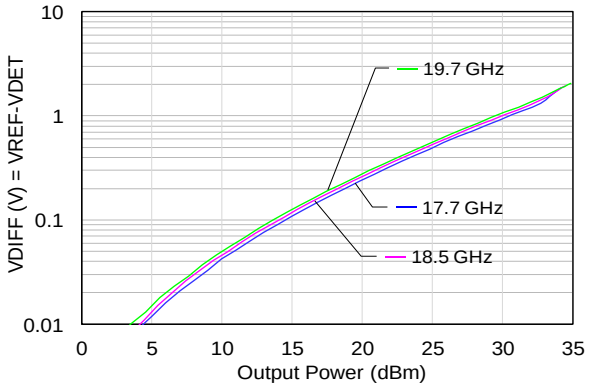
Performance Plots

Test conditions unless otherwise noted: Temp. = 25 °C, V_D = 6 V, I_{DQ} = 1430 mA, V_G = -0.7 V typical

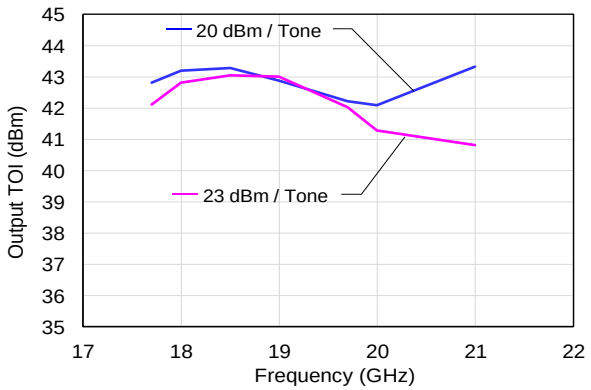
Power Added Efficiency vs. Frequency



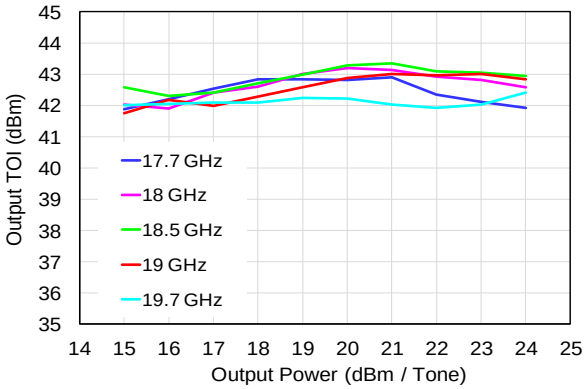
Power Detector vs. Output Power vs. Frequency



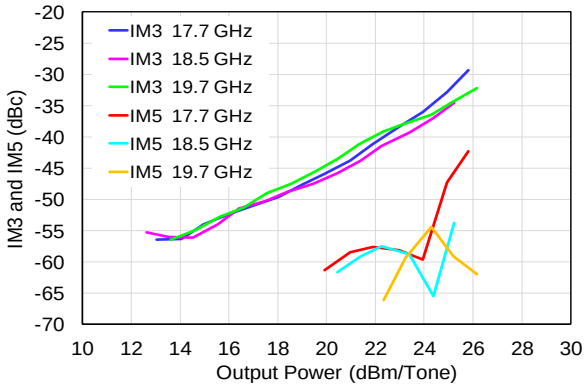
Output TOI vs. Frequency vs. Output Power / Tone



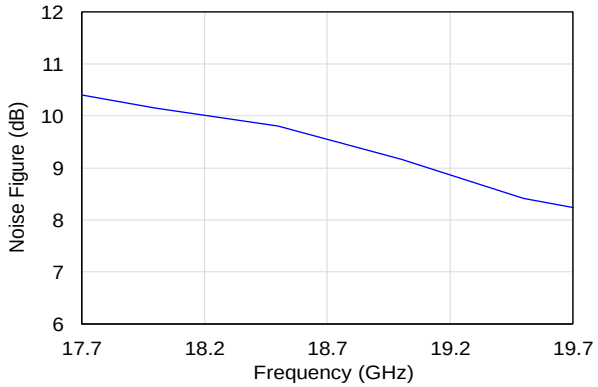
Output TOI vs. Output Power / Tone



IM3 and IM5 vs. Output Power / Tone vs. Frequency



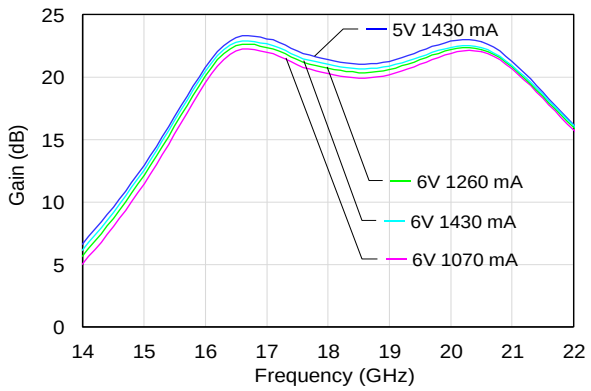
Noise Figure vs. Frequency



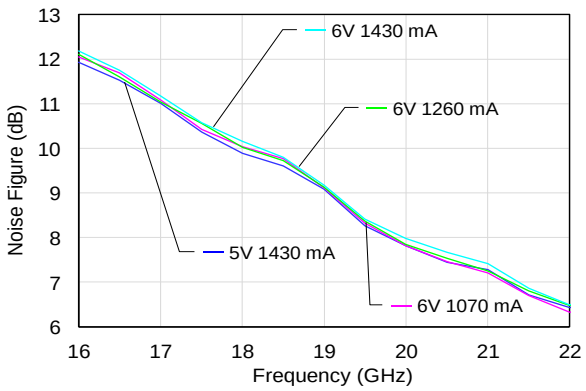
Performance Plots

Test conditions unless otherwise noted: Temp. = 25 °C, V_D = 6 V, I_{DQ} = 1430 mA, V_G = -0.7 V typical

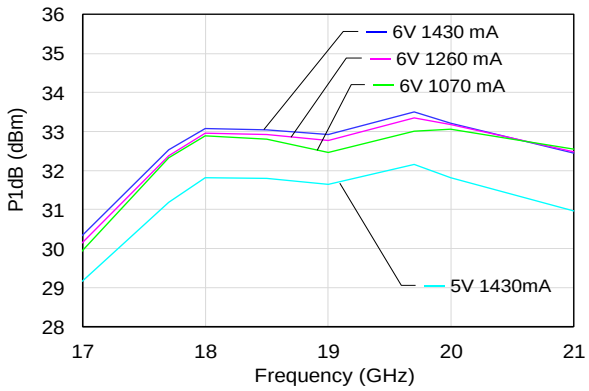
Gain vs. Frequency vs. Bias



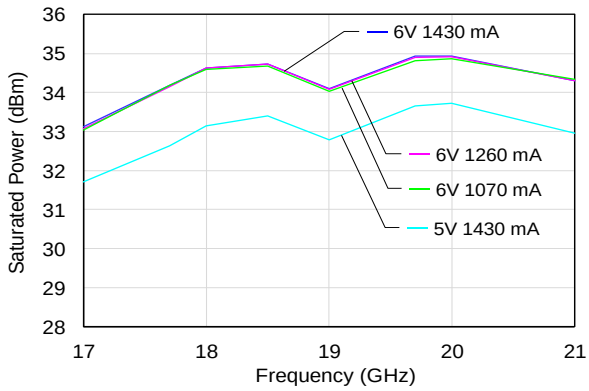
Noise Figure vs. Frequency vs. Bias



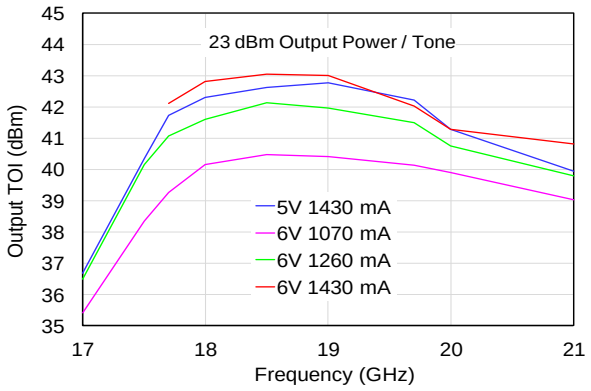
P1dB vs. Frequency vs. Bias



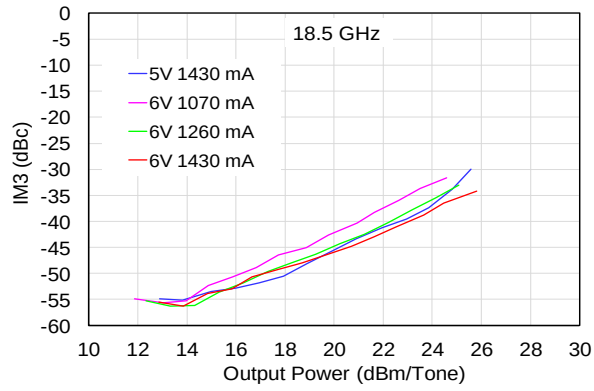
Saturated Power vs. Frequency vs. Bias



Output TOI vs. Frequency vs. Bias



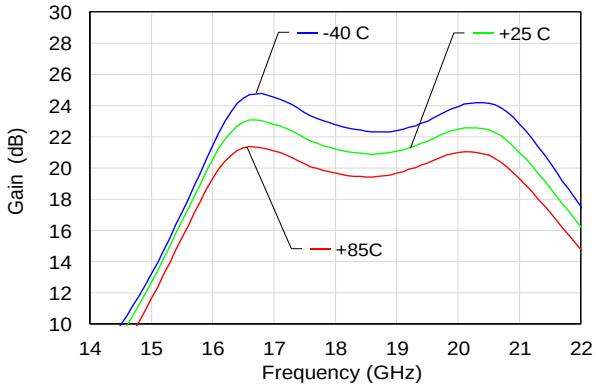
IM3 vs. Output Power / Tone vs. Bias



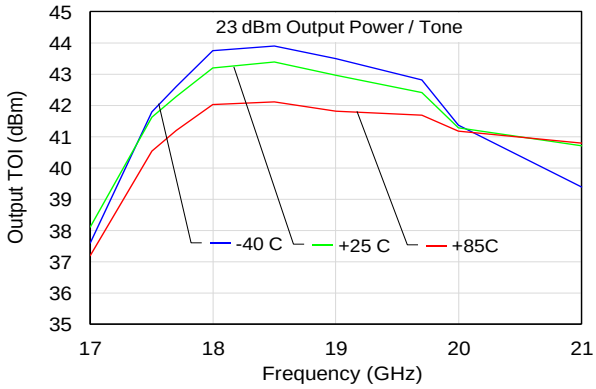
Performance Plots

Test conditions unless otherwise noted: Temp. = 25 °C, V_D = 6 V, I_{DQ} = 1430 mA, V_G = -0.7 V typical

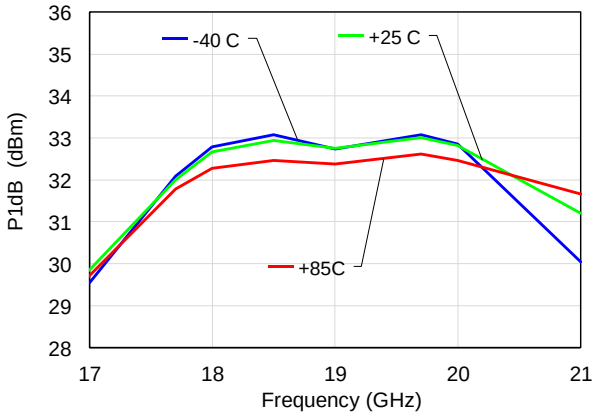
Gain vs. Frequency vs. Temperature



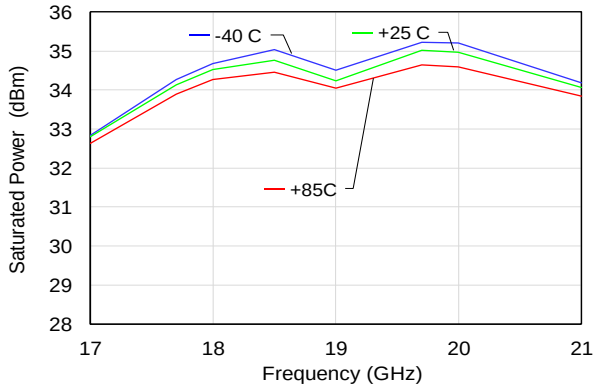
Output TOI vs. Frequency vs. Temperature



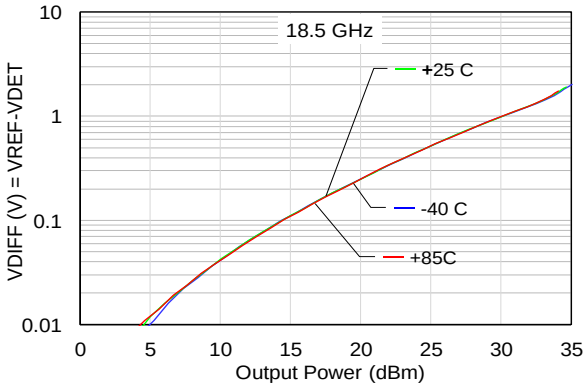
P1dB vs. Frequency vs. Temperature



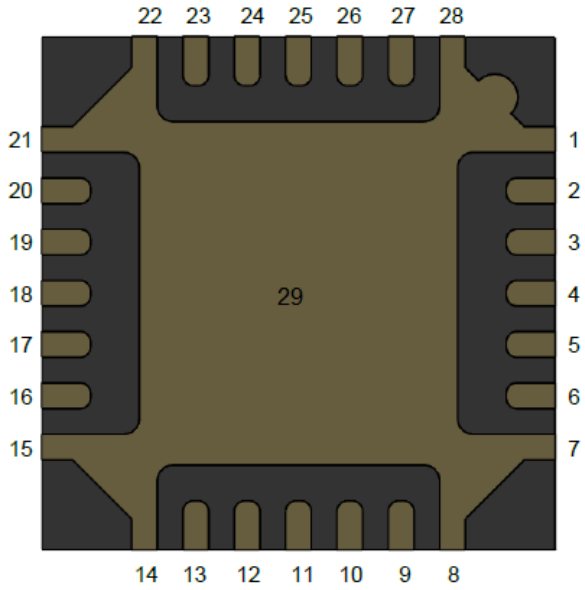
Saturated Power vs. Frequency vs. Temperature



Power Detector vs. Output Power vs. Temperature



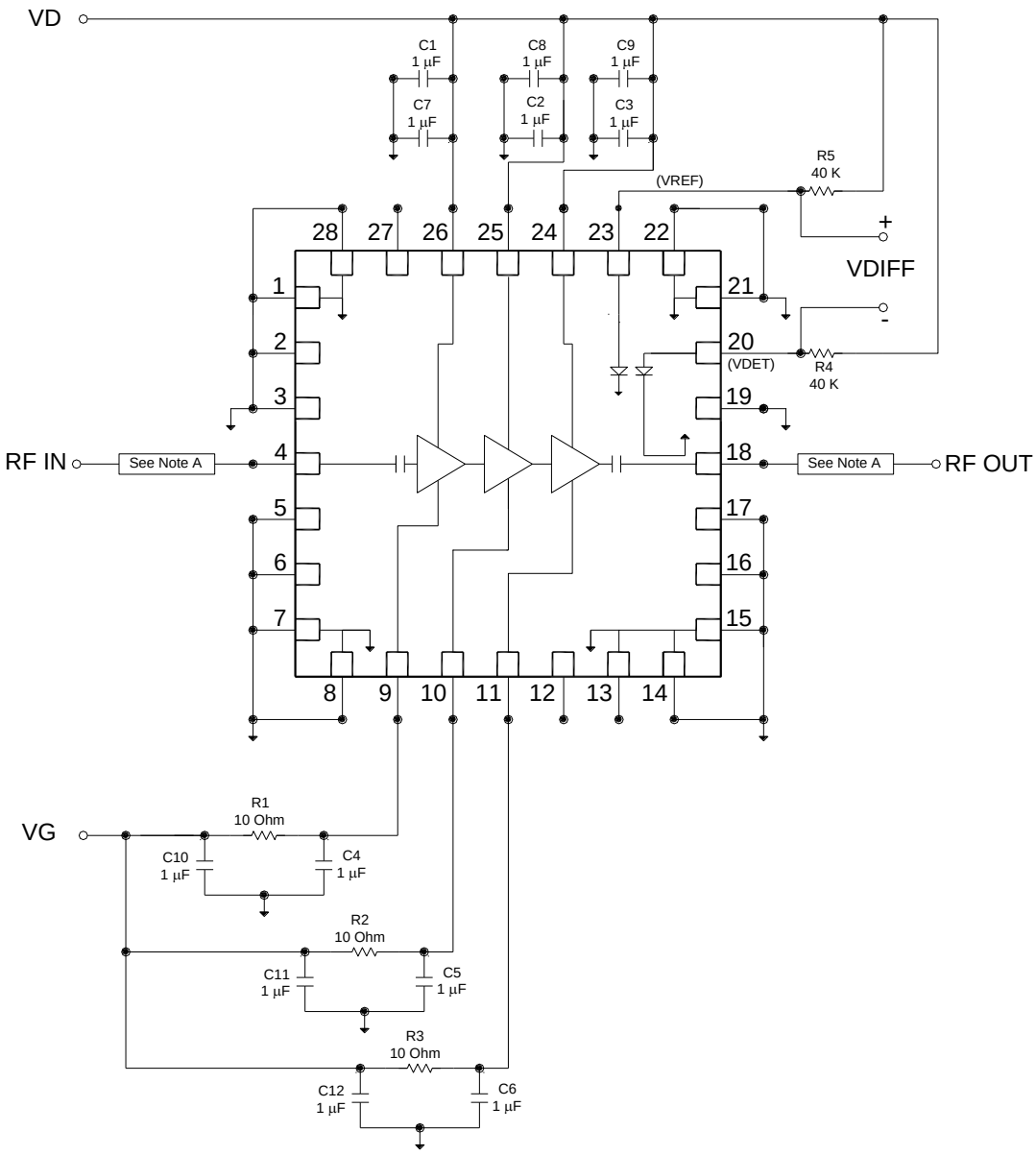
Pin Configuration and Description



Pin No.	Label	Description
1,7,8,14,15,21,22,28,29	GND	Backside paddle. Multiple vias should be employed to minimize inductance and thermal resistance; see 'PCB Mounting Pattern' on page 10 for suggested footprint
2,3,5,6,16,17,19	N/C	No internal connection; Recommend grounding these pins for best RF performance. See 'PCB Mounting Pattern' on page 10 for suggested footprint
4	RF IN	RF input, matched to 50 ohms
9	VG1	Stage 1 gate voltage (1)
10	VG2	Stage 2 gate voltage (1)
11	VG3	Stage 3 gate voltage (1)
12, 27	N/C	No internal connection; May be grounded on PCB or left open
13	GND	Internally connected to GND. May be grounded on the PCB or left open
18	RF OUT	RF output, matched to 50 ohms
20	VDET	Detector diode output voltage. Varies with RF output power
23	VREF	Reference diode output voltage
24	VD3	Stage 3 drain voltage (1)
25	VD2	Stage 2 drain voltage (1)
26	VD1	Stage 1 drain voltage (1)

(1) Bias bypass network is required; see 'Application Circuit' on page 8 as an example

Applications Circuit



Note A: 50 Ω Microstrip Transmission Line.

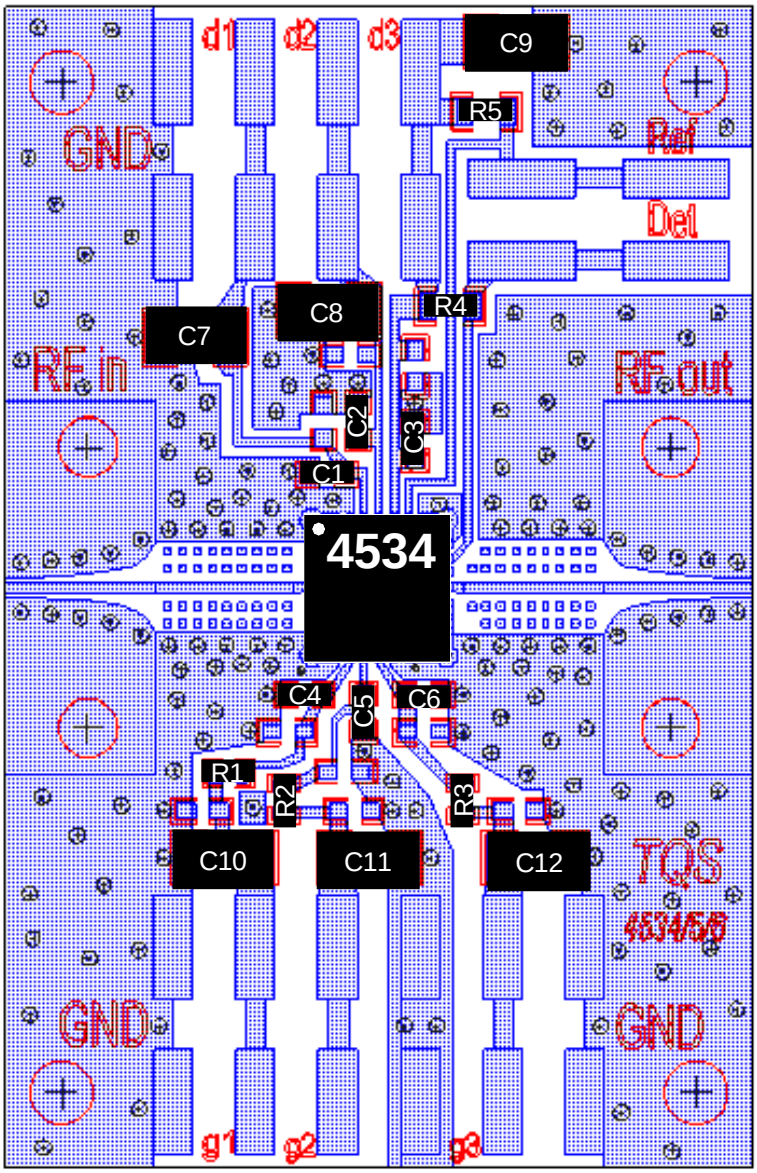
Bias Up Procedure

1. Set I_D limit to 2800 mA, I_G limit to 60 mA
2. Set V_G to −1.5 V
3. Set V_D +6 V
4. Adjust V_G more positive until I_{DQ} = 1430 mA (V_G ~ −0.4 V to -0.8 V typical range)
5. Apply RF signal

Bias Down Procedure

1. Turn off RF signal
2. Reduce V_G to −1.5 V. Ensure I_{DQ} ~ 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Evaluation Board Layout

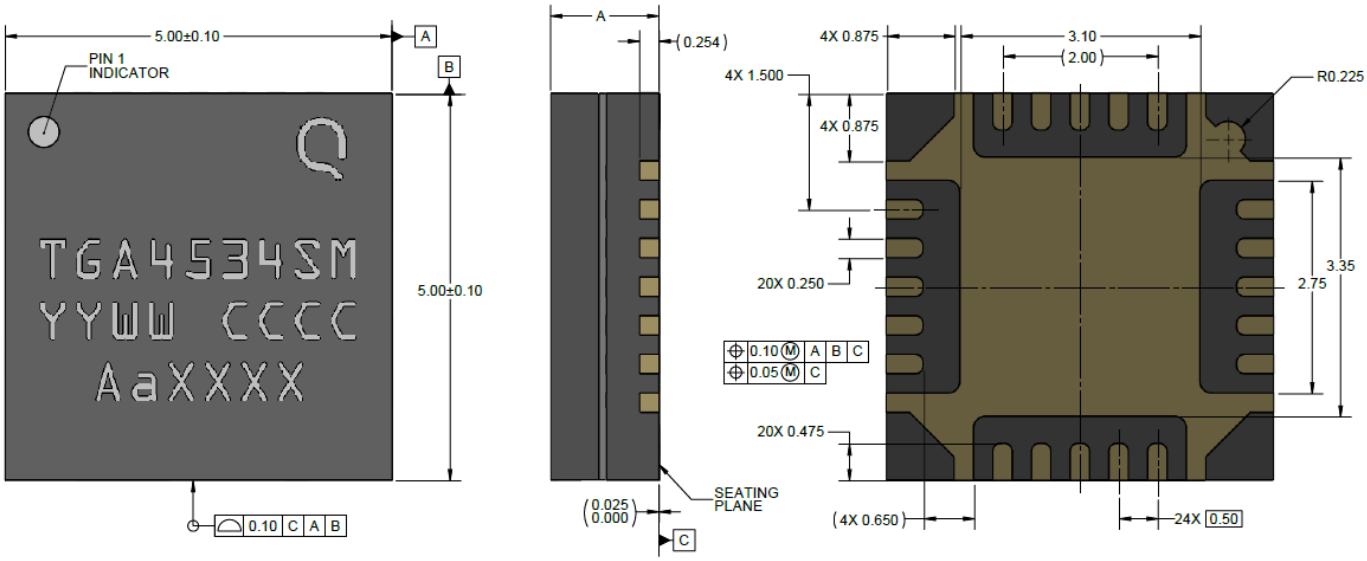


Board material is Rogers Corp. 4003 0.008" thickness with ½ oz copper cladding.
For further technical information, refer to the TGA4534-SM Product Information page.

Bill of Material

Ref. Des.	Value	Description	Manuf.	Part Number
U1		K Band Power Amplifier	Qorvo	TGA4534-SM
C1 thru C6	1.0 µF	Cap, 0402, 25 V, 10%, X5R SMD	Various	
C7 thru C12	1.0 µF	Cap, 0805, 25 V, 10%, X5R SMD	Various	
R1, R2, R3	10 Ω	Res, 0402, 0.06 W, 5%, SMD	Various	
R4, R5	40 kΩ	Res, 0402, 0.06 W, 5%, SMD	Various	

Package Marking & Dimensions

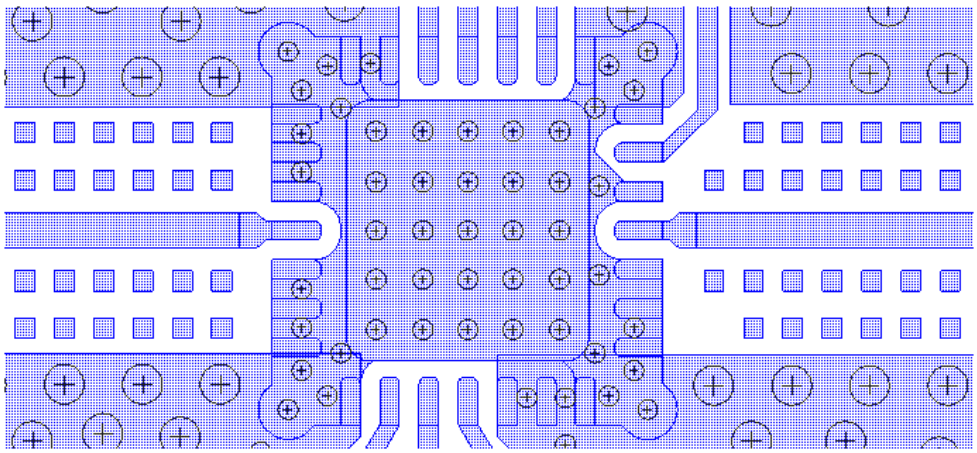


LASER MARK NOTES:
- YY IS THE LAST TWO DIGITS OF THE CALENDAR YEAR AND WW IS THE WEEK NUMBER OF THE ASSEMBLY LOT START.
- CCCC IS COUNTRY CODE.
- Aa IS VENDOR (AC).
- XXXX IS THE BATCH ID.

		ACSLP
A	MAX.	1.400
	NOM	1.300
	MIN.	1.200

NOTES: UNLESS OTHERWISE SPECIFIED;
1. PACKAGE LEADS ARE GOLD PLATED.

PCB Mounting Pattern



Notes:

1. The pad pattern shown has been developed and tested for optimized assembly at Qorvo. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.
2. Ground vias are critical for the proper performance of this device. Vias have a final plated thru diameter of .25 mm (.010”).

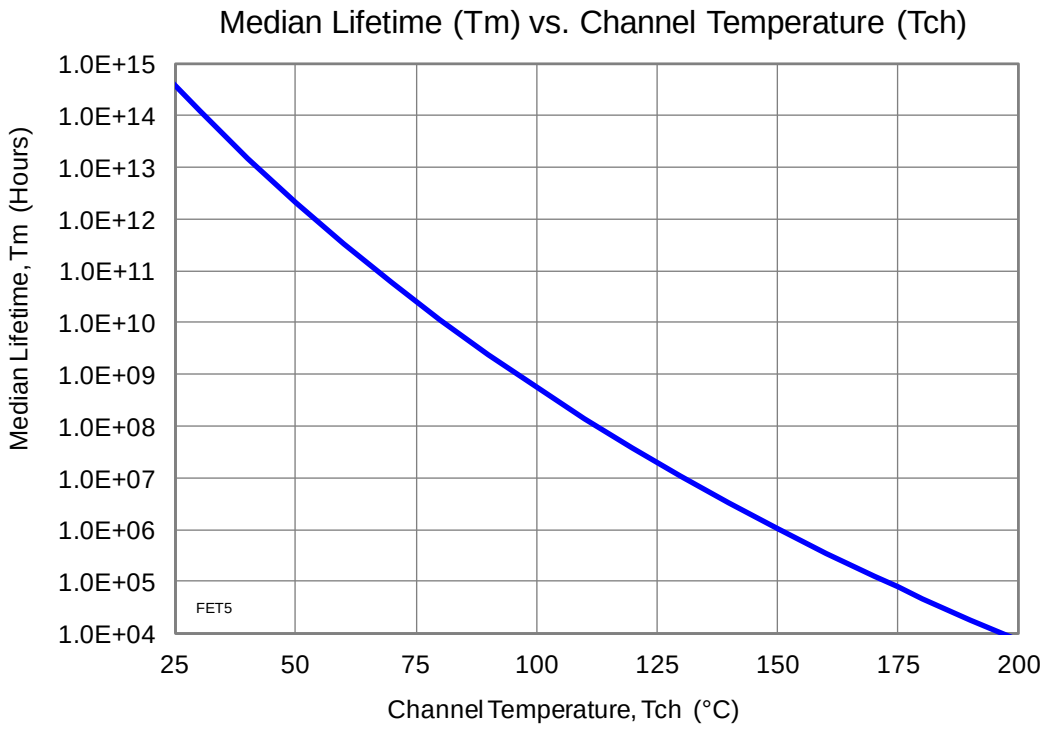
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85°C, V_D = 6 V, I_{DQ} = 1430 mA P_{DISS} = 8.6 W	5.75	°C/W
Channel Temperature (T_{CH}) (No RF Drive)		134	°C
Median Lifetime (T_M)		6.6E+6	Hrs
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85°C V_D = 6 V, I_{DD} = 2100 mA P_{OUT} = 34.2 dBm, P_{DISS} = 10 W	5.75	°C/W
Channel Temperature (T_{CH}) (Under RF Drive)		143	°C
Median Lifetime (T_M)		2.4E+6	Hrs

Notes:
1. Thermal resistance is measured to back of the package.

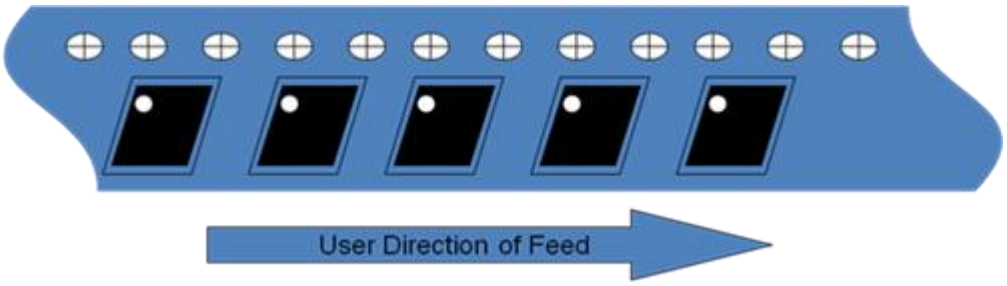
Median Lifetime

Test Conditions: V_D = 6 V
Failure Criteria = 10% reduction in I_{D_MAX}



Tape and reel Information

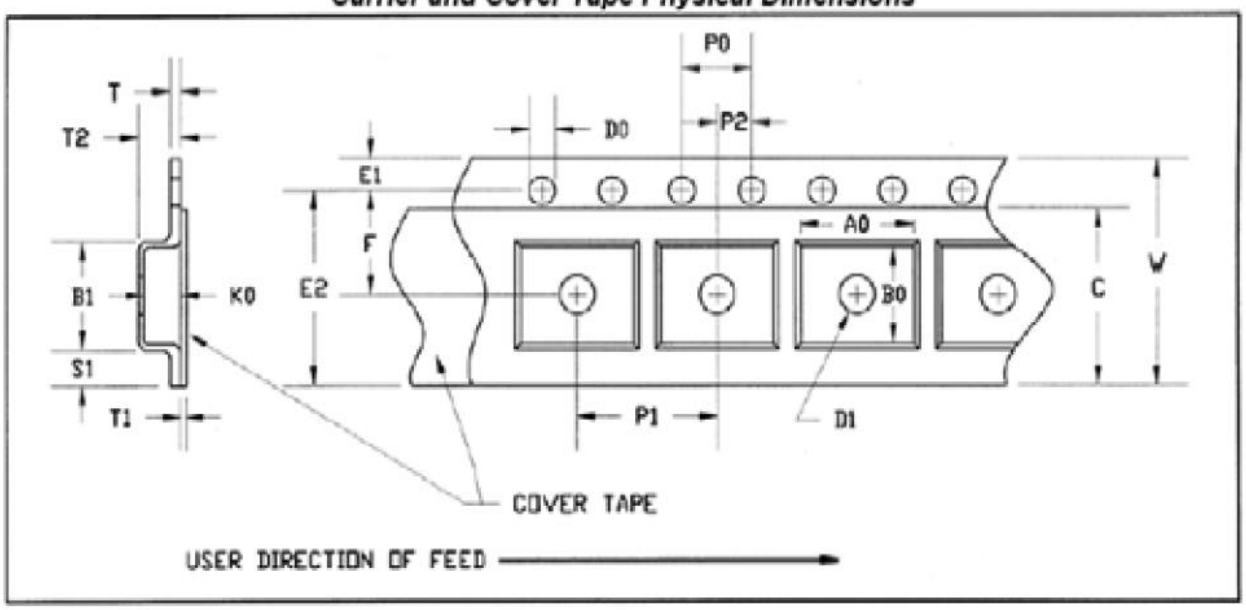
Standard T/R size = 500 pieces on a 7” reel



CARRIER AND COVER TAPE DIMENSIONS

Part	Feature	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.209	5.3
	Width	B0	0.209	5.3
	Depth	K0	0.065	1.65
	Pitch	P1	0.314	8
Centerline Distance	Cavity to Perforation – Length Direction	P2	0.079	2
	Cavity to Perforation – Width Direction	F	0.217	5.5
Cover Tape	Width	C	0.362	9.2
Carrier Tape	Width	W	0.472	12

Carrier and Cover Tape Physical Dimensions



Solderability

Compatible with lead-free soldering processes with 260°C peak reflow temperature.

This package is air-cavity and non-hermetic, and therefore cannot be subjected to aqueous washing. The use of no-clean solder to avoid washing after soldering is highly recommended.

Contact plating: Ni-Au

Solder rework not recommended

Recommended Soldering Temperature Profile